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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GERARD CHAUVEL, SERGE LASSERRE,
and DOMINIQUE D'INVERNO

Appeal 2008-005101
Application 10/632,216
Technology Center 2100

Decided:[1] July 2, 2009

Before HOWARD B. BLANKENSHIP, JAY P. LUCAS, and
THU A. DANG, *Administrative Patent Judges*.

DANG, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

I. STATEMENT OF CASE

Appellants appeal the Examiner's final rejection of claims 1-23 under 35 U.S.C. § 134(a) (2002). We have jurisdiction under 35 U.S.C. § 6(b)(2002).

We AFFIRM.

A. INVENTION

According to Appellants, the invention relates generally to processors and more particularly to the use of "micro-sequences" in the efficient of code such as Bytecodes (Spec. 3, [0002]).

B. ILLUSTRATIVE CLAIM

Claims 1 and 10 are exemplary and are reproduced below:

1. A processor, comprising:

fetch logic that retrieves instructions from memory;

decode logic coupled to said fetch logic, the decode logic decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set; and

an active program counter selected as either a first program counter or a second program counter;

wherein an instruction of the first instruction set is replaced by a micro-sequence comprising one or more instructions of the second instruction set and the active program counter switches between the first and second program counters based on a micro-sequence-active bit.

10. A method, comprising:

fetching an instruction; and

determining whether said instruction is to be executed or replaced by a group of other instructions, the determining independent of the type of the instruction.

C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Greenberger	US 6,092,179	Jul. 18, 2000
Gee	US 6,317,872 B1	Nov. 13, 2001
Zaidi	US 6,581,154 B1	Jun. 17, 2003
Seal	US 6,965,984 B2	Nov. 15, 2005

Claims 10-14 stand rejected under 35 U.S.C. § 112, first paragraph as lacking enablement and failing to comply with written description requirement;

Claims 1-4, 7-9, 19, and 20 stand rejected under 35 U.S.C. § 103(a) over the teachings of Seal in view of Gee;

Claims 5 and 6 stand rejected under 35 U.S.C. § 103(a) over the teachings of Seal in view of Gee and Zaidi;

Claims 10 and 13 stand rejected under 35 U.S.C. § 102(e) as anticipated by the teachings of Gee;

Claims 10-12, 14, 22, and 23 stand rejected under 35 U.S.C. § 103(a) over the teachings of Zaidi;

Claims 15-17 stand rejected under 35 U.S.C. § 103(a) over the teachings of Seal in view of Gee and Greenberger; and

Claims 18 and 21 stand rejected under 35 U.S.C. § 103(a) over the teachings of Seal.

II. ISSUES

The issues are whether Appellants have shown that the Examiner erred in determining that:

1) the limitation "independent of the type of the instruction" (claim 10) is not described in the Specification in such a way as to enable one skilled in the art to make and/or use the invention, and fails the written description requirement;

2) Seal, in view of Gee, teaches and/or would have suggested a decode logic that "decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set" (claim 1);

3) Gee teaches "determining whether said instruction is to be executed or replaced by a group of other instructions" (claim 10); and

4) Zaidi teaches or would have suggested "determining whether said instruction is to be executed or replaced by a group of other instructions" (claim 10).

III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Seal

1. Seal discloses a bytecode translation hardware which receives Java bytecodes to generate a sequence of corresponding ARM instructions, that are then passed to the processor core (col. 6, ll. 10-17; Fig. 1).
2. The bytecode translation hardware maps a simple Java bytecode to a sequence of corresponding ARM instructions that may be executed by the processor core (*id.*, ll. 17-20).
3. As there are 256 possible bytecode values, the table of pointers contains 256 pointers, and up to 256 ARM native instruction code fragments are provided to perform the processing specified by all possible Java bytecodes (col. 7, ll. 4-9; Fig. 2).

Gee

4. Gee discloses instruction bytecodes fetched from code memory and stored in an instruction register, wherein execution begins with the translation of the opcode portion of the bytecode into a starting microprogram address and a microsequencer causes proper execution of the instruction (col. 8, l. 63 to col. 9, l. 4).
5. A control store contains microinstruction sequences for each of the JAVA bytecodes (col. 9, ll. 5-21).

Zaidi

6. Zaidi discloses converting special micro-operation (Suop) into one or more micro-ops (uops) containing a code sequence that will perform

the particular variant of the set of multiple variant macro-instructions as specified by the macro-instruction (col. 2, ll. 7-14).

7. The processor executes the instructions contained in the uop or Suop (col. 3, ll. 41-43).

IV. PRINCIPLES OF LAW

35 U.S.C. § 112, 1st paragraph

"The specification shall contain a written description of the invention… in such full, clear, concise, and exact terms as to enable any person skill in the art to which it pertains, or with which it is most nearly connected, to make and use the same" 35 U.S.C. § 112, first paragraph.

35 U.S.C. § 102

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citation omitted). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) "In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art." *Id.* (citations omitted).

The *claims* measure the invention. *See SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). "[T]he PTO gives

claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

Of course, anticipation "is not an 'ipsissimis verbis' test." *In re Bond*, 910 F.2d 831, 832-33 (Fed. Cir. 1990) (citing *Akzo N.V. v. United States Int'l Trade Comm'n*, 808 F.2d 1471, 1479 n.11 (Fed. Cir. 1986)). "An anticipatory reference . . . need not duplicate word for word what is in the claims." *Standard Havens Prods., Inc., v. Gencor Indus., Inc.,* 953 F.2d 1360, 1369 (Fed. Cir. 1991).

35 U.S.C. § 103

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007).

The test for obviousness is rather what the combined teachings of the references would have suggested to those of ordinary skill in the art. *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981); *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991).

V. ANALYSIS

Claims 10-14 under 112, 1st paragraph

The Examiner finds that claims 10-14 contain subject matter which was not described in the Specification in such a way as to enable one skilled in the art to make and/or use the invention because "[t]here is no existence of working examples of a determining step in the specification that is independent of the type of the instruction" since "bit 168 is set of cleared directly dependent on the type of the instruction" (Ans. 22). The Examiner further finds that claims 10-14 fail to comply with the written description requirement because, in the Specification, "determining if the instruction is to be replaced is directly dependent on the type of instruction accessing the table" (Ans. 24).

Appellants contend that the Specification at page 13, paragraph [0030] "discloses that the decode logic fetches a Bytecode instruction from an instruction storage, then the decode logic uses the Bytecode as an index into the vector table to examine the associated bit" (App. Br. 10). Accordingly, Appellants contend that Specification shows that "the determination whether the Bytecode is to be replaced is made independent of the type of Bytecode fetched from memory" (*id.*).

The issues we address on appeal are whether claim 10, which recites "the determining independent of the type of the instruction," lacks enablement and whether the claim complies with the written description requirement.

As to whether claim 10 lacks enablement, as the Appellants contend, the Specification "discloses that the decode logic fetches a Bytecode

instruction from an instruction storage, then the decode logic uses the Bytecode as an index into the vector table to examine the associated bit" (App. Br. 10). We agree that such disclosure in the Specification enables one skilled in the art to make and/or use the invention. As such, we conclude that Appellants have shown that the Examiner erred in concluding that claims 10-14 lack enablement.

As to whether claim 10 complies with the written description requirement, the Examiner finds that "[a] type of the instruction is described in paragraph 25 of the specification as being determined upon decoding," and "a type of the instruction is interpreted as including parts of the instruction that identify what and how the instruction is to operate" (Ans. 4). Thus, the Examiner finds that "the type of the instruction must be taken into consideration when determining which bytecodes will be replaced by a micro-sequence and what the address will be to point to this sequence of instructions" (Ans. 5).

Though Appellants contend that the Specification "discloses that the decode logic fetches a Bytecode instruction from an instruction storage, then the decode logic uses the Bytecode as an index into the vector table to examine the associated bit" (App. Br. 10), we find no written description in the Specification to indicate that the associated bit is independent of the type of the instruction. That is, while we find that the determination to replace the Bytecode is dependent on the associated bit, we find no written description that the associated bit is independent of the type of Bytecode.

Accordingly, we agree with the Examiner that the Specification does not contain a written description of the invention in full, clear, concise, and exact terms as required by under 35 U.S.C. § 112, first paragraph.

Therefore, though Appellants have shown that the Examiner erred in concluding that claims 10-14 lack enablement, Appellants have not shown that the Examiner erred in concluding that claims 10-14 fail to comply with written description requirement under 35 U.S.C. § 112, first paragraph.

Claims 1-4, and 7-9 over Seal in view of Gee

As to claim 1, Appellants argue that "Seal appears to teach a decoder 10 that can decode only ARM instructions" and "Seal's bytecode translation hardware 6 operates only on Java bytecodes" (App. Br. 14). Thus, Appellants contend that "the references still fail to teach or fairly suggest a 'decode logic… decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set'," because "the system is provided either Java bytecodes or ARM instructions, but not a mixture" (*id.*).

However, the Examiner finds that "[p]redecoding the incoming instructions or bytecodes prior to either the JAVA bytecodes being received by the translation hardware or the ARM instructions being received by the decoder would be one of the finite solutions" and that "[t]his allows for detecting JAVA bytecodes in order to set flag 21 or detecting ARM instructions to clear flag 21 in the processor of Seal (Ans. 26). Thus, the

issue that we address on appeal is whether Seal, in view of Gee, teaches and/or would have suggested a decode logic that "decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set" (claim 1).

We begin our analysis by giving the claims their broadest reasonable interpretation. *See In re Bigio,* 381 F.3d at 1324. Furthermore, our analysis will not read limitations into the claims from the specification. *See In re Van Geuns,* 988 F.2d at 1184.

Though Appellants argue that "the system is provided either Java bytecodes or ARM instructions, but not a mixture" (App. Br. 14), Appellants appear to be arguing that the references do not disclose providing a mixture of JAVA bytecodes and ARM instructions *at the same time*. However, claim 1 does not recite any such "at the same time" language, and such argument is not commensurate with the language of claim 1. In fact, claim 1 does not place any limitation or context on what the "decode logic" means, includes, or represents other than that the decode logic decodes instructions from "a first instruction set and a second instruction set." Thus, we will not limit the decode logic to an entity that decodes a mixture of instructions from a "first instruction set" and a "second instruction" *at the same time*, as Appellants contend. Instead, we broadly interpret claim 1 as an entity for decoding instructions from first and second sets, wherein the information is provided from the two sets at any time.

Seal discloses providing Java bytecodes to generate a sequence of corresponding ARM instructions, and then providing the ARM instructions to the processor core (FF 1). In fact, Appellants admit that Seal teaches decoding ARM instructions and operating on Java bytecodes (App. Br. 14). We find that an artisan would have understood that Seal does provide a mixture of Java bytecodes and ARM instructions. That is, the system of Seal does decode both Java bytecodes and ARM instructions, wherein Java bytecodes are different from ARM instructions.

Accordingly, we agree with the Examiner that Seal, in view of Gee, would have suggested a decode logic that "decodes instructions from a first instruction set and a second instruction set, the second instruction set different than the first instruction set" as required by claim 1. We conclude that the Appellants have not shown that the Examiner erred in rejecting independent claim 1 under 35 U.S.C. § 103(a). Appellants do not provide separate arguments with respect to the rejection of claims 3, 4, and 7-9 depending therefrom. Thus, we conclude that the Appellants also have not shown that the Examiner erred in rejecting claims 3, 4, and 7-9, under 35 U.S.C. § 103(a).

As to claim 2, Appellants further contend that "Seal appears to teach a table of pointers pointing to ARM code fragments, but the table does not include information which indicates whether the Java bytecode is to be replaced by the ARM code fragments" (App. Br. 15). However, Seal discloses mapping a simple Java bytecode to a sequence of corresponding

ARM instructions (FF 2), wherein the table of pointers is used to point the ARM instruction code fragments to perform the processing specified by possible Java bytecodes (FF 3). We find that it would have understood by skilled artisans that the mapping of the Java bytecodes to the ARM code fragments in Seal would include information which indicates whether the Java bytecode is to be replaced by the ARM code fragments. That is, an artisan would have understood the table of pointers of Seal to be a vector table which includes information which specifies whether an instruction is to be replaced by a micro-sequence, as required by claim 2.

Thus, we agree with the Examiner that Seal in view of Gee also would have fairly suggested the limitations of claim 2. Accordingly, Appellants also have not shown that the Examiner erred in rejecting claim 2 under 35 U.S.C. § 103(a).

Claims 5 and 6 over Seal in view of Gee and Zaidi

Claims 5 and 6 depend from claim 1. Appellants contend that "[c]laims 5 and 6 are allowable for at least the same reasons [as claim 1]" (App. Br. 16). As discussed above with respect to claim 1, we agree with the Examiner that the combination of Seal and Gee. Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 5 and 6 depending therefrom over the combination of Seal and Gee and further in view of Zaidi under 35 U.S.C. § 103(a).

Claims 10 and 13 over Gee

Appellants argue that "Gee fails to inherently or expressly teach 'determining whether said instruction is to be executed or replaced by a group of other instructions'" since "in accordance with Gee it is not required to decide whether to replace the fetched bytecode as the bytecode is always replaced by a group of other instructions" (App. Br. 17). Though the Examiner agrees that, in Gee, "every bytecode is replaced by a sequence of mincroinstructions" (Ans. 27), the Examiner responds that "Gee disclosed that the processor makes a determination that all macroinstructions are to be replaced by a sequence of microinstructions instead of directly executing the macroinstructions" (*id.*). An issue that we address on appeal is whether Gee expressly or inherently teaches "determining whether said instruction is to be executed or replaced by a group of other instructions" (claim 10).

Gee discloses executing instructions, wherein a control store contains microinstruction sequences for each of the JAVA bytecodes (FF 4-5). As Appellants contend and the Examiner agrees, in Gee, "every bytecode is replaced by a sequence of microinstructions" (App. Br. 17 and Ans. 27). However, though the Examiner responds with "Gee disclosed the claimed limitation" (Ans. 27), in the section relied by the Examiner in Gee, there is no teaching of *determining whether or not* an instruction is to be executed or replaced.

Accordingly, we conclude that the Appellants have shown that the Examiner erred in rejecting claim 10 and claim 13 depending therefrom over Gee under 35 U.S.C. § 102(e).

Claims 10-12, 14, 22, and 23 over Zaidi

Appellants contend that "Zaidi teaches Suops as merely a way of representing multiple Uops and are not themselves executable," and thus "Zaidi fails to teach or fairly suggest that a 'fetching an instruction; and determining whether said instruction is to be executed or replaced by a group of other instructions'" (App. Br. 19). However, the Examiner finds that "there is no requirement in the claims that the instruction fetched that is replaced with a sequence of instructions must itself be capable of execution on the processor" (Ans. 27), and that "[t]he Suop is an instruction that is to be replaced by a sequence of instructions" (*id.*). Thus, the issue that we address on appeal is whether Zaidi teaches or would have suggested "determining whether said instruction is to be executed or replaced by a group of other instructions" (claim 10).

Though Appellants argue that the instructions "are not themselves executable" (App. Br. 19), claim 10 does not place any limitation or context on what "instruction" means, includes, or represents other than that the instruction is determined "to be executed *or* replaced by a group of other instructions." That is, giving the claims their broadest reasonable interpretation without reading limitations into the claims from the

Specification, we interpret that claim 10 merely requires that the instruction is executed *or* replaced by a group of other instructions.

Zaidi discloses converting Suop into one or more micro-ops (uops) containing a code sequence (FF 6). An artisan would have understood such conversion of Suop into micro-ops to be replacing the Suop by a group of other instructions. That is, Zaidi discloses determining whether to replace an instruction with a group of other instructions, as required by claim 10.

Furthermore, Zaidi discloses that the processor executes the instructions contained in the uop or Suop (FF 7). Thus, even if claim 10 requires that the instruction to be replaced must be an executable instruction, Zaidi discloses that the Suop to be replaced is executable by the processor. An artisan would have understood such processor of Zaidi determines whether the Suop is to be executed or the uops replacing the Suop is to be executed.

Accordingly, we agree with the Examiner that Zaidi would have suggested "determining whether said instruction is to be executed or replaced by a group of other instructions," as required by claim 10. We conclude that the Appellants have not shown that the Examiner erred in rejecting independent claim 10 and claims 11, 12, 14, 22, and 23 grouped therewith under 35 U.S.C. § 103(a) over Zaidi.

Claims 15-17 over Seal in view of Gee and Greenberger

As to claims 15 and 17, Appellants repeat that "the references still fail to teach or fairly suggest that a 'decode logic coupled to said fetch logic, the decode logic decodes instructions from a first instruction set and the second instruction set'" (App. Br. 20). As discussed above with respect to claim 1 which recites a similar feature, we agree with the Examiner that the combination of Seal and Gee teaches and strongly suggests such claimed feature.

Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claim 15 and 17 over the combination of Seal and Gee, and further in view of Greenberger, under 35 U.S.C. § 103(a).

As to claim 16, Appellants repeat the contention that "Seal appears to teach a table of pointers accessible by the Java translation hardware 6; however, the table of pointers does not include information which indicates whether the Java bytecode are to be replaced by the ARM code fragments" (App. Br. 21). However, as discussed above regarding claim 2 which recites a similar feature, Seal discloses mapping a simple Java bytecode to a sequence of corresponding ARM instructions (FF 2), wherein the table of pointers is used to point the ARM instruction code fragments to perform the processing specified by possible Java bytecodes (FF 3). Skilled artisans would have understood the table of pointers of Seal to be a vector table comprising entries which includes a field indicating whether the Java bytecode is to be replaced by ARM instructions. In particular, an artisan

would have understood that the table indicates whether the corresponding instruction is to be executed by the processor *or* whether the instruction is to be replaced by a micro-sequence, as required by claim 16.

Thus, we agree with the Examiner that Seal in view of Gee and Greenberger also would have fairly suggested the limitations of claim 16. Accordingly, Appellants also have not shown that the Examiner erred in rejecting claim 16 under 35 U.S.C. § 103(a).

Claims 18 and 21 over Seal, and claims 19 and 20 over Seal and Gee

As to claims 18 and 21, Appellants repeat that Seal "fails to teach or fairly suggest 'decode logic that decodes instructions, the decode logic decodes instructions from a first instruction set and a second instruction set'" (App. Br. 22). As discussed above with respect to claim 1 which recites similar feature, we agree with the Examiner that Seal teaches and strongly suggests such claimed feature.

Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 18 and 21 therefrom over Seal under 35 U.S.C. § 103(a).

Appellants do not provide separate arguments for claims 19 and 20 depending from claim 18. Accordingly, we conclude that the Appellants have not shown that the Examiner erred in rejecting claims 19 and 20 over Seal in view of Gee under 35 U.S.C. § 103(a).

VI. CONCLUSIONS

(1) Appellants have shown that the Examiner erred in concluding that claims 10-14 lack enablement, but have not shown that the Examiner erred in concluding that claims 10-14 fail to comply with written description requirement under 35 U.S.C. § 112, first paragraph.

(2) Appellants have not shown that the Examiner erred in finding that claims 1-4, 7-9, 19, and 20 are unpatentable over the teachings of Seal and Gee.

(3) Appellants have not shown that the Examiner erred in finding that claims 5 and 6 are unpatentable over the teachings of Seal, Gee, and Zaidi.

(4) Appellants have shown that the Examiner erred in finding that claims 10 and 13 are anticipated by the teachings of Gee.

(5) Appellants have not shown that the Examiner erred in finding that claims 10-12, 14, 22, and 23 are unpatentable over the teachings of Zaidi.

(6) Appellants have not shown that the Examiner erred in finding that claims 15-17 are unpatentable over the teachings of Seal, Gee, and Greenberger.

(7) Appellants have not shown that the Examiner erred in finding that claims 18 and 21 are unpatentable over the teachings of Seal.

(8) Claims 1-23 are not patentable over the prior art of record.

VII. DECISION

We reverse the Examiner's decision rejecting claims 10 and 13 under 35 U.S.C. § 102(e). However, we affirm the Examiner's decision rejecting claims 10-14 under 35 U.S.C. § 112, 1st paragraph, and rejecting claims 1-12 and 14-23 under 35 U.S.C. § 103(a).

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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